CLAIMS

[0069] What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A pixel cell comprising:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the photo-generated charge under control of a control gate, and

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring photo-generated charge from the photo-conversion device to the charge storage region.

2. The pixel cell of claim 1, wherein the charge storage region is part of a buried channel MOS capacitor.

3. The pixel cell of claim 1, wherein the charge storage region is below a surface of the substrate.

4. The pixel cell of claim 1, wherein the charge storage region comprises:

a doped region of a second conductivity type; and

a doped surface layer of a first conductivity type over and in contact with the doped region of a second conductivity type, the control gate being over the doped surface layer.

5. The pixel cell of claim 1, wherein the control gate comprises polysilicon doped with a first conductivity type dopant.

6. The pixel cell of claim 1, wherein the first transistor is a shutter transistor for determining an integration time for the pixel cell.

7. The pixel cell of claim 1, further comprising:

a sensing node; and

a second transistor having its gate between the charge storage region and the sensing node.

8. The pixel cell of claim 7, wherein the sensing node is a floating diffusion region.

9. The pixel cell of claim 7, wherein the control gate at least partially overlaps the first and second transistor gates.

10. The pixel cell of claim 1, wherein the photo-conversion device is a pinned photodiode.

11. A pixel cell comprising:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the photo-generated charge under control of a control gate, wherein the charge storage region comprises a doped region of a second conductivity type and a doped surface layer of a first conductivity type over and in contact with the doped region of a second conductivity type, and wherein the control gate is over the doped surface layer; and

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring photo-generated charge from the photo-conversion device to the charge storage region.

12. The pixel cell of claim 11, wherein the charge storage region is part of a buried channel metal oxide semiconductor (MOS) capacitor.

13. The pixel cell of claim 11, further comprising:

a sensing node; and

a second transistor having its gate between the charge storage region and the sensing node.

14. The pixel cell of claim 13, wherein the control gate overlaps the first and second transistor gates.

15. An image sensor comprising:

a substrate;

an array of pixel cells formed on the substrate, wherein each pixel cell comprises:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the photo-generated charge under control of a control gate, and

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring photo-generated charge from the photo-conversion device to the charge storage region.

16. The image sensor of claim 15, wherein the charge storage region is part of a buried channel metal oxide semiconductor (MOS) capacitor.

17. The image sensor of claim 15, wherein the charge storage region comprises:

a doped region of a second conductivity type;

a doped surface layer of a first conductivity type over and in contact with the doped region of a second conductivity type, the control gate being over the doped surface layer.

18. The image sensor of claim 15, wherein the control gate comprises polysilicon doped to a first conductivity type.

19. The image sensor of claim 15, wherein the first transistor is a shutter transistor for determining an integration time for the pixel cell.

20. The image sensor of claim 15, further comprising:

a sensing node; and

a second transistor gate of a second transistor between the charge storage region and the sensing node.

21. The image sensor of claim 20, wherein the control gate at least partially overlaps the first and second transistor gates.

22. A processor system, comprising:

(i) a processor; and

(ii) an image sensor coupled to the processor, the image sensor comprising:

a substrate;

a pixel formed over the substrate, the pixel comprising:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the photo-generated charge under control of a control gate, and

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring photo-generated charge from the photo-conversion device to the charge storage region.

23. An integrated circuit comprising:

a substrate;

an array of pixel cells at a surface of the substrate, wherein at least one of the pixel cells comprises a photo-conversion device that generates charge, a gate controlled charge storage region that stores the photo-generated charge under control of a control gate, and a first transistor having its gate between the photo-conversion device and the charge storage region for transferring photo-generated charge from the photo-conversion device to the charge storage region;

circuitry coupled to the array, wherein the circuitry comprises a conductive line coupled to the control gate, the conductive line providing signals to the control gate.

24. A method of forming a pixel cell, the method comprising:

forming a photo-conversion device that generates charge;

forming a gate controlled charge storage region that stores the photo-generated charge;

forming a control gate that controls the charge storage region, and

forming a first transistor having its gate between the photo-conversion device and the charge storage region for transferring photo-generated charge from the photo-conversion device to the charge storage region.

25. The method of claim 24, wherein the acts of forming the charge storage region and control gate comprise forming a buried channel metal oxide semiconductor (MOS) capacitor.

26. The method of claim 24, wherein the act of forming the charge storage region comprises forming the charge storage region below a surface of the substrate.

27. The method of claim 24, wherein the act of forming the charge storage region comprises:

forming a doped region of a second conductivity type; and

forming a doped surface layer of a first conductivity type over and in contact with the doped region of a second conductivity type, and wherein the act of forming the control gate comprises forming the control gate over the doped surface layer.

28. The method of claim 24, wherein the act of forming the control gate comprises forming a layer of polysilicon doped with a first conductivity type dopant.

29. The method of claim 24, wherein the act of forming the first transistor comprises forming a shutter transistor for determining an integration time for the pixel cell.

30. The method of claim 24, further comprising:

forming a sensing node; and

forming a second transistor gate of a second transistor between the charge storage region and the sensing node.

31. The method of claim 30, wherein the act of forming the sensing node comprises forming a floating diffusion region.

32. The method of claim 30, wherein the act of forming the control gate comprises forming the control gate at least partially overlapping the first and second transistor gates.

33. The method of claim 24, wherein the act of forming the photo-conversion device comprises forming a pinned photodiode.

34. A method of forming a pixel cell, the method comprising:

forming a photo-conversion device for generating charge;

forming a doped region of a second conductivity type spaced apart from the photo-conversion device;

forming a doped surface layer of a first conductivity type over the doped region of a second conductivity type;

forming a gate of a first transistor between the photo-conversion device and the doped region of a second conductivity type; and

forming a gate electrode over the doped surface layer.

35. The method of claim 34, further comprising:

forming a sensing node; and

forming a gate of a second transistor between the doped region of a second conductivity type and the sensing node.

36. The method of claim 35, wherein the act of forming the gate electrode over the doped surface layer comprises forming the gate electrode overlapping the first and second transistor gates.

37. A method for operating a pixel cell, the method comprising:

generating charge in response to light during an integration period;

transferring the photo-generated charge to a gate controlled charge storage region by operating a gate of a first transistor and operating a control gate that controls the charge storage region; and

storing the photo-generated charge in the charge storage region until a time for readout by operating the control gate.

38. The method of claim 37, wherein the act of storing the photo-generated charge comprises storing the photo-generated charge below a surface of a substrate.

39. The method of claim 37, further comprising determining the length of the integration period for the pixel cell by operating the gate of the first transistor.

40. The method of claim 37, further comprising transferring the photo-generated charge from the charge storage region to a sensing node by operating the control gate and operating a gate of a second transistor.

41. The method of claim 40, wherein the act of transferring the photo-generated charge to the sensing node comprises transferring the photo-generated charge to a floating diffusion region.

42. The method of claim 40, further comprising reading out the photo-generated charge by applying a voltage on the sensing node to a readout circuit.

43. A method of operating an image sensor, the method comprising:

generating charge in response to incident light concurrently within a plurality of pixel cells during an integration time;

transferring the photo-generated charge to gate controlled charge storage regions within respective pixel cells simultaneously by operating gates of shutter transistors and operating control gates that control the charge storage regions;

storing the photo-generated charge in the charge storage regions until a time for readout by operating the control gates;

at a time for readout of a first pixel cell, transferring photo-generated charge from a first charge storage region to a first sensing node by operating a gate of an associated first transistor;

sampling a value of the first sensing node;

at a time for readout for a second pixel cell, transferring photo-generated charge from a second charge storage region to a second sensing node by operating a gate of an associated second transistor;

sampling a value of the second sensing node; and

processing the values to obtain an image.

44. The method of claim 43, wherein the act of generating charge comprises generating charge within all pixel cells of an array concurrently.

45. The method of claim 44, wherein the act of transferring the photo-generated charge to a plurality of storage regions comprises transferring the photo-generated charge to charge storage regions within all pixel cells of an array concurrently.